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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,720	09/09/2003	Toshikazu Kato	N27180702E	2771

7590 12/29/2004

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,720	KATO, TOSHIKAZU	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-14* is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/09/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated November 26, 2004, Applicant has elected without traverse Group I (claims **1-14)** and canceled claims **15-20**, and Fig. 10 of the drawings has been amended to include the label of Prior Art is acknowledged. Accordingly, claims **1-14** are currently pending in the application.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in JAPAN, 2002-271807 on 09/18/2002.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 09/09/03 and made of record as Paper No. 09/09/03. The references cited on the PTOL 1449 form have been considered.

Claim Objections

Claims **5 and 6** are objected to because of the following reasons.

In line 1, "the least'' should read –the at least--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Christensen et al. (USP 5,889,306 hereinafter referred to as "Christensen") in view of Wyborn et al. (USP 5,587,339 hereinafter referred to as "Wyborn").

Regarding claims **1 and 3**, Christensen discloses in Figs. 7-9 and the corresponding texts as set forth in column 3, line 15-column 5, line 30, a semiconductor device comprises:

an insulator layer 14 formed on and extending over a semiconductor substrate 12; and

a plurality of element regions 32A, 32B formed over the insulator layer separated from one another and having at least one circuit element 25A formed therein, each element region being in contact with the insulator layer.

Christensen does not teach or suggest the semiconductor device comprises a low resistance embedded wiring layer formed on and extending over the semiconductor substrate.

Wyborn teaches in Fig. 5 a semiconductor device comprises an aluminum or aluminum alloy interconnect layer 2 extending over a dielectric layer 4 which itself extends over a silicon substrate 6, and aluminum or aluminum alloys are widely used to form a low resistance interconnect layer in semiconductor devices as set forth in column 1, lines 53-5, and column 3,

lines 10-15, the semiconductor device further includes an insulating layer 4 formed between the embedded wiring layer/the low resistance aluminum or aluminum alloy interconnect layer and the semiconductor substrate; the embedded wiring layer/the low resistance aluminum or aluminum alloy interconnect layer is electrically connected to the semiconductor substrate through at least one opening 8 in the insulating layer; and the semiconductor substrate receives a predetermined power source potential.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a low resistance aluminum or aluminum alloy interconnect layer extending over a silicon substrate, as taught by Wyborn to incorporate into Christensen's structure to arrive the claimed limitation in order to provide low resisitivity contacts (col. 5, line 16).

Regarding claim **2**, Christensen discloses in Figs. 8-9 the plurality of element regions includes at least one supply element region 34 in contact with the embedded wiring layer and receiving a predetermined power source potential.

Regarding claims **4 and 5**, Christensen discloses in Figs. 7-9 the semiconductor device wherein the at least one circuit element includes a transistor 25A having a source region 30A, drain region 30B, and channel region 32A formed in the element region, the channel region being situated between each of the source and drain regions and the embedded wiring layer; and the other of the source and drain regions being electrically connected to the embedded wiring layer.

Regarding claim **6**, Christensen discloses in Figs. 7B and 8B the semiconductor device wherein the at least one circuit element includes a transistor 25A having a source region 28A, drain region 28B, and channel region 32A formed in the element region, the element region

being surrounded by at least one insulating layer 18 except for a bottom portion thereof, the source and drain regions being in contact with the at least one insulating layer and not in contact with the embedded wiring layer.

Allowable Subject Matter

Claims **7-14** are allowed. The following is a statement of reason for the indication of allowable subject matter:

Claims **7-14** are considered allowable since the prior art of record fails to teach or render obvious a semiconductor device comprises, in combination with all other features, a low resistance first embedded wiring layer and a low resistance second embedded wiring layer both formed on and extending over a semiconductor substrate, the first embedded wiring layer supplied with a first potential and the second embedded wiring layer supplied with a second potential different than the first potential as recited in independent claim **7**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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12/24/04

Andy Huynh

Patent Examiner